Department of
ELECTRONICS AND COMMUNICATION ENGINEERING

A Report on
5 Day Workshop on Automation of Digital Logics Using HDL's
(18th July to 22nd July 2023)

Department of ECE successfully conducted a five day workshop on **"Automation of Digital Logics Using HDL's"** for II B.Tech students on **18th July to 22nd July 2023**. The aim of this workshop is to provide an insight on basics of digital logic designs which are used for Digital VLSI design using the Verilog HDLs. The workshop comprises of theoretical lectures delivered by department faculty and also hands on live demonstration of EDA tools for digital design.

The students will have an exposure to Artix-7 FPGA, Zynq-7000 SoC, Xilinx Vivado ML Enterprise tool for digital design, verification and synthesis. After completion of workshop, the students will be able to **design, verify,** and **synthesize** the digital circuits using HDLs and advanced FPGAs.

Total 35 students were registered for the workshop and participation certificate for all 35 were issued by the college.

Dr. B. HariPrasad Naik and **Mr. A. Aravind,** worked as Faculty Coordinators for the five day workshop.

Day-1:

The workshop was inaugurated by Dean, School of Engineering and Head of the Department, ECE at 10 am.

Dr. S. Ravi Chand, HOD-ECE addressed the gathering

Dr. B. Hari Prasad Naik, Convener of workshop addressed the gathering

Prof. P.S. Sreenivas Reddy, CoE-NNRG addressed the gathering

In the morning session, Mr. A.Aravind as resource person delivered the “Basic concepts of Modeling the Digital Circuits”. Afternoon session, “Implementation of Basic Digital Logics was performed using Verilog HDL” in Xilinx Vivado.

Mr. A. Aravind, Asst. Prof. as resource person delivered the concepts of "Basic concepts of Modeling the Digital Circuits"

Implementation of Digital Circuits is done in Verilog HDL using Xilinx Vivado Simulation tool.

Day-2:

In morning session, resource person N.Lavanya delivered the theoretical session on "Design of combinational logic circuits with applications".

Afternoon session, "Hand's on Implementation of Combinational Logic Circuits" such as full adder, decoder and encoder was performed using Xilinx Vivado in Verilog HDL"

Mrs. N. Lavanya, Asst. Prof. as resource person delivered the concepts of "Design of combinational logic circuits with applications".

"Hand's on Implementation of Combinational Logic Circuits"

Day-3:

In morning session, resource person A.Aravind delivered theoretical design lecture on "Sequential logic circuits".

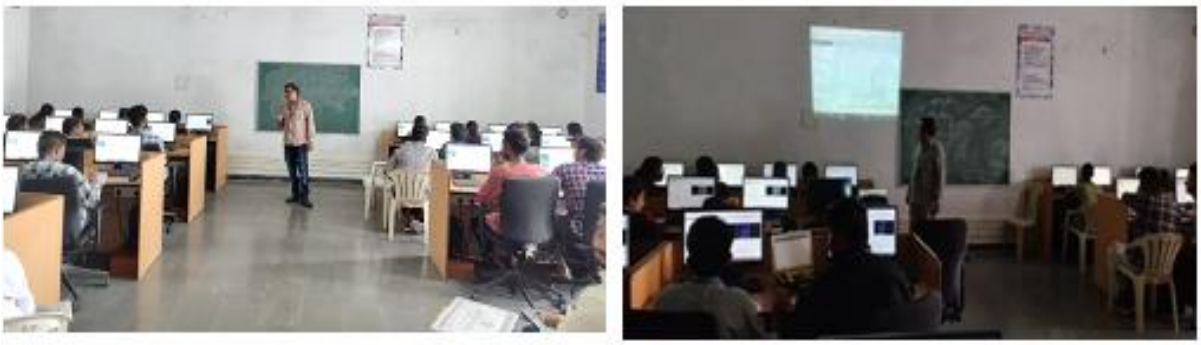
Afternoon session, implementation of "Sequential Logic Circuits" such as flip-flops, counter and shift register is performed using Xilinx Vivado in Verilog HDL".

Hands on implementation of "Sequential Logic Circuits"

Day-4:

In morning session, resource person Dr.V.Sravan Kumar delivered a lecture on "Artix-7 FPGA development board and Zynq-7000 series SoC boards" descriptions.

Afternoon session, "Implementation of Adder-Compressor Block Design" was performed using Xilinx Vivado on the target Artix-7 FPGA and Zynq-7000 series SoC boards.



Dr.V.Sravan Kumar delivered a lecture on "Artix-7 FPGA development board and Zynq-7000 series SoC boards"

Day-5:

In morning session, resource person Dr.B.HariPrasad Naik delivered a lecture on "Automation of Digital Logics using IP Cores" on the target Artix-7 FPGA and Zynq-7000 series SoC boards".


Dr.B.HariPrasad Naik delivered a lecture on "Automation of Digital Logics using IP Cores"

Finally, the workshop ended with a valedictory session, in the presence of Director Dr.C.V.Krishna Reddy garu and Head of Department Dr. S.Ravi Chand. Student participants received their certificates from the Director, Dr.C.V.Krishna Reddy.

Workshop Participants with HOD, Convener and Faculty

Workshop Participants with Director,HOD, Convener and Faculty

Student Participant is receiving Certificate from Director Dr. C.V. Krishna Reddy .

Converner of workshop Dr. B. Hari Prasad Naik is receiving Appredciation Certificate from the Director Dr. C. V. Krishna Reddy.

Convener of Workshop with his team

HOD-ECE with Convener of Workshop and team

Workshop Participants with HOD, Convener and Faculty.

Outcome's of the Workshop:

After the completion of workshop, the students were able to

- Understand the basic modeling of digital logic design.
- Design the various digital logics using the Verilog HDL.
- Implement and verify the digital logics using IP cores on advanced FPGA's.

Place: Hyderabad
Date: 25/07/2023

Convener **HOD-ECE**